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09/503,122	02/14/2000	Leon Saltsov	WH-10752US	6124

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EXAMINER

SHAPIRO, JEFFERY A

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.



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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 23

Application Number: 09/503,122
Filing Date: February 14, 2000
Appellant(s): SALTSOV ET AL.

MAILED

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GROUP 3600

S. Warren Hall
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/23/02.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

Appellant's brief includes a statement that claims 1-6, 8, and 10-20 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

6,241,069 B1	Mazur et al	6-2001
5,964,336	Itako et al	10-1999
6,142,284	Saltsov	11-2000
6,079,018	Hardy et al	6-2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Meyer et al.
2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazur et al (US 6,241,069) in view of Meyer et al.
3. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazur et al (US 6,241,069) in view of Itako et al.
4. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazur et al (US 6,241,069) in view of Meyer et al and further in view of Itako et al.
5. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over US 6,142,284 in view of Meyer et al.

These rejections are set forth in prior Office Action, Paper No. 6.

(11) Response to Argument

Applicant asserts that the prior art cited in the above rejections are “incompatible, fail to teach or suggest the combination, and in addition, even if improperly combined, do not result in the structure as claimed.”

As described in the final rejection, as well as the arguments below, this appears to not be the case. On the contrary, it appears that the cited prior art reads on Applicant’s claims based upon a reasonably broad interpretation of said claims.

Applicant’s system is described as a banknote validator, concisely described as having a discriminator which determines characteristics of the banknote and a memory which contains information and programs, such as characteristic, image and property information on a particular denomination of banknote. The memory which Applicant uses for this is a flash-type memory. Such a memory is a nonvolatile-type of memory. The flash-type memory that the Applicant uses is embodied in a removable module which may be exchanged with another module and “plugged” into an appropriate connector within the “validator” itself.

Mazur et al discloses a currency handling system with a validator. Specifically, as described in the final office action, the system of Mazur et al has a channel for processing a banknote (note the rollers and belts which take the bill from hopper (18)), a series of sensors (42) located along the channel (see figure 8), a central processing unit (CPU)(1610), and a memory storage arrangement (82), which appears to be illustrated as removable, in figure 10. Note that memory module (82) fits into socket (84) in the circuit board (88). The description of figure 10 under the brief description of drawings mentions this removability aspect of the memory module as well.

Meyer et al generally discloses a central processing unit (1) in a pay-phone system which evaluates the integrity of any memory storage arrangement in col. 16, lines 60-67 and col. 17, lines 1-35 and 61-63. The fact that it is a telephone arrangement or even that the system incorporates a network/LAN is immaterial to the idea of using testing procedure to evaluate the integrity of a new removable flash memory module inserted in connection with the system. Both Meyer et al and Mazur et al are systems which handle currency and discern currency using a validator. This is how these systems work. However, the important item is that the flash memory module of Meyer et al evaluates the integrity of the module in the system. Even whether or not the flash memory of Meyer et al is actually removable makes no difference, since Mazur et al clearly teaches such a feature. Simply because a reference provides more features than Applicant's claim limitations does not preclude its use in rejecting said claim limitations. Mazur et al has such a removable module. Therefore, it would stand to reason that one ordinarily skilled in the art would take the teaching of Meyer et al and use such evaluation routines in the removable flash modules of Mazur et al. Meyer et al also includes remote downloading/uploading of data, records and operation program codes, as stated in the abstract. Motivation/suggestions are as cited in the final office action.

Itako et al also describes a system which uses a bill validator having removable sensors. It would be obvious for one of ordinary skill in the art to use the teaching of Itako et al in the system of Meyer et al to periodically replace the sensors of the system so as to maintain the security of the system and prevent counterfeit currency being passed through the system. Itako et al states this motivation/suggestion in col. 2, lines 25-31.

Whether or not the primary reference requires two-way communication or not, it would be obvious to one ordinarily skilled in the art to take a flash card module, place it in one computer, update the software or data, etc., and then hand carry it to a system and place it in the machine interface. In fact, in the context of Applicant's claims, it can be argued that these are functional equivalents of each other.

Applicant asserts that one of the major differences between Applicant's system and the system of the prior art is that the removable memory arrangement is located in the "validator" module. However, whether or not this is true, they are, at the very least, functional equivalents of each other. Further more, what does one define as the validator module? The sensor and the memory, the sensor and the memory and the cpu? It can be argued that the validator module is just an encasement of variety of working parts, and that the number of parts contained in the validator is arbitrary and design choice based upon the required need to make certain parts contained together for removal for, say, maintenance purposes. At the extremes, a validator could include only a sensor, or could encompass the sensor, the memory, the cpu, the coin box, and each and every part of the machine which uses the validator, such as a vending machine or pay-phone.

Applicant states that "the validator conducts its own evaluation of the integrity of the removable flash memory module based on information provided to it by the removable flash memory module." However, what information? Programs? Pattern data? Even ID data is information. With a reasonable and broad reading of the Claims, it appears that even the passing of identification of the flashcard by ID or serial number information would be the same as or a functional equivalent of identifying the flashcard by a particular program or pattern data. It is

well-known to those ordinarily skilled in the art that a system must identify the flashcard in some manner, otherwise the flashcard can not attach to the system and be used as an incorporated part of the system. Also, note that even if the mother board's DS2502 is inherent only to telephone systems, the problem solved is recognition of a particular circuitry, which is the same problem in matching a flash card module as described in Mazur et al, to a motherboard, as shown in Mazur et al at figure 10.

Regarding US Patent 6,142,284 it is noted that the described prior art provides the necessary teachings and motivation required for maintenance of the double patenting rejection described in the final action.

As such, Claims 1-6, 8 and 10-20 should be rejected based upon the prior art cited. Note also that any mention of rejection of Canceled Claims 7 or 9 was in error, and should not be included as they have been effectively cancelled per amendment dated 11/19/01. Finally, IDS dated 9/20/2001 has been considered on 4/29/03, a copy of which is enclosed with this Examiner's Answer for Applicant's records.

Regarding the remand of 3/24/04, note that the 112 rejection of the prior final rejection has been withdrawn. Claims 16-20 are rejected under 35 U.S.C. Sec, 103 over Mazur in view of Meyer and further in view of Itako. This rejection is maintained, above. Applicant's new arguments regarding Meyer are believed to have been dealt with previously in the "Response to Arguments" section.

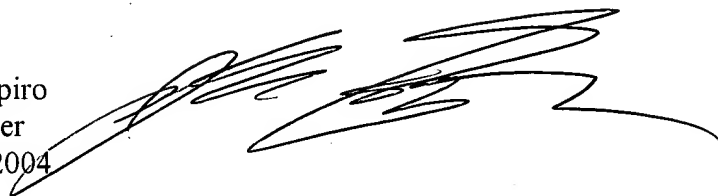
For the above reasons, it is suggested that the rejections should be sustained.

Application/Control Number: 09/503,122
Art Unit: 3653

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Respectfully submitted,

Jeffrey A. Shapiro
Patent Examiner
November 8, 2004

A handwritten signature in black ink, appearing to read 'Jeffrey A. Shapiro', written over the printed name and date.

Conferees

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